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(54) **Data distribution network.**

(57) In a mainsborne control system, part of the electrical mains supply 1 services individual consumers in separate houses 2, 3 and 4 (shown by broken lines). The mains circuit 5, within each house, in connected to a number of electrical appliances, e.g. lights 6, 7, 8, thermostats 9, 10 and electric fire 11. Each appliance has an associated interface unit 6' etc (but only shown for 6). Each house has a controller 12 13 and 14 respectively, to generate and send selectively control signals to any appliance in that house by suitable coding of the signal. The code signal is a stream of digits divided into elements forming pairs of digits, each digit having one of three carrier states. Each digit pair is permitted to have only some of the possible permutations such that the existence of any other permutation in a signal indicates that that signal has been corrupted.

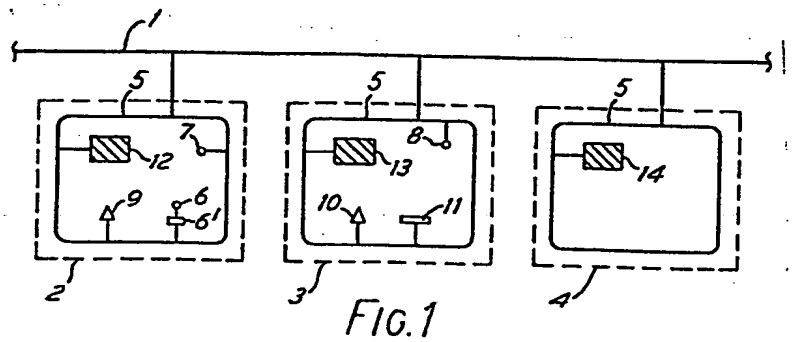

FIG. 1

EP 0 120 640 A2

DATA DISTRIBUTION NETWORK

The present invention relates to a data distribution network particularly but not exclusively a broadband local area network, and to equipment for use with a network.

In a broadband local area network with multiple access from separate transmitters, it is possible that two different data signals will collide during transmission thereby causing corruption of the data. Also a data signal may be corrupted by spurious other signals on the network. Corruption of either type can have unfortunate consequences particularly when the network is a mains-borne control system for a building.

An object of the invention is to provide a network which utilizes signals having a readily-identifiable characteristic which changes upon combination of signals.

The present invention provides a data distribution network having a pathway along which information signals can be sent and a plurality of stations, interconnected by the pathway, for reception and/or transmission of information signals, the network having means to generate a digital signal for transmission with the network, said signal being formed of a plurality of elements of which at least some are each formed of one of a number of predetermined permutations of multiple-state digits, whereby the combination of two or three different such permutations does not result in any of those predetermined

permutations, at least one of the stations having means to detect whether an element in a signal has one of the predetermined permutations.

Within the context of this patent specification, the term "multiple-state digit" means that the digit has one state out of a given number of possible states in the way that a "binary-state" digit has one state out of two possible states and a "ternary-state" digit has one state out of three possible states.

Thus by investigating whether the relevant elements of a signal upon arrival at its destination has one of the predetermined permutations, one can determine whether it has been involved in a collision during transmission.

Preferably, the relevant elements in the signal are pairs of digits.

In one form of the invention, an element is formed of any one of predetermined permutations of ternary-state digits. Thus each digit can have any one of three carrier states, namely "high frequency carrier", "no carrier" and "low frequency carrier". Also preferably there are only three predetermined permutations which are permitted i.e. upon generation the signal is composed of elements of only three permitted permutations. Thus any signal detected at a later stage having an element of any permutation other than one of those three must have been involved in a collision. This choice of numbers of digits in an element and numbers of predetermined permutations provides high level of protection without excessive redundancy of information.

Preferably the at least one of the stations has means to block any signal which has an element without one of the predetermined permutations. Also the network may have means to determine what part of the signal contains the element and means to identify whether the permutation of the elements is a predetermined one; it may also have means to send information on the identified permutation to a central control unit for the

network. Furthermore it may have means to determine the original composition, before collision of data signals which have been detected as including permutations other than the predetermined ones.

The present invention also provides an encoder capable of forming a digital signal having a plurality of elements of which at least some are each formed of one of a number of predetermined permutations of multiple-state digits, whereby the combination of two or three different such permutations does not result in any of these predetermined permutations.

Furthermore, the present invention also provides a signal-collision detector comprising means to identify the state held by each part of an element in a signal, and means to determine whether the permutation of the states within an element is a predetermined permutation.

The present invention is particularly suitable for a mains-borne control system (within a flat or house and/or between them) but clearly it is not restricted to that application. Thus it can also be used in a broadcast network or in a network with a transmission line whose principal function is the sending of the data signals. The transmission line can be formed of any one or more suitable mediums e.g. metallic wire or optical fibre.

In another form of the invention, an element is formed of any one of predetermined permutations of binary-state digits. This may provide a reduction in the installation costs of such a network in that there need only be a single carrier frequency, i.e. the two carrier states are "carrier" and "no carrier".

In another form of the invention, an element is formed of any one of predetermined permutations of quarternary-state digits. While this may provide a reduced protection against errors, it allows a higher rate of information transfer and is easier to implement. There can be added to this form of the invention error protection by providing, for example, cyclic redundancy checks or "check-sums".

In any of the forms of the invention the number of permitted permutations can be changed.

In order that the invention may more readily be understood, a description is now given, by way of example only, reference being made to the accompanying drawings in which:

Figure 1 is a schematic diagram of a network embodying the present invention;

Figure 2 is a representation of the three permitted permutations of ternary states for an element.

Figure 3 shows the composition of a signal packet for use in the network of Figure 1.

Figure 4 shows an appliance for use in the network of Figure 1.

Figures 5 and 6 illustrate an encoder and a decoder, respectively, for the network of Figure 1.

In the mains-borne control system shown schematically in Figure 1, part of the electrical mains supply 1 services individual consumers in separate houses 2, 3 and 4 (shown by broken lines). The mains circuit within each house is represented as a loop 5, to which there are connected a number of electrical appliances, eg. lights 6, 7, 8, thermostats 9, 10 and electric fire 11. Each appliance has an associated interface unit 6' etc (but shown only for 6). Each house 2, 3 and 4 has a controller 12, 13 and 14 respectively, which can generate and send selectively control signals to any of those appliances in that house by suitably coding the signal to designate the appropriate recipient. The signal can effect any of the following operations as required: turning the appliance on or off; varying the power input to the appliance, eg. to dim or brighten a light or to turn a fire up or down; instructing the appliance to reply to a particular question eg. to determine the states of the appliance or to measure a variable (eg. local temperature). However, a controller (eg. 12) in a house 2 is not capable of generating a control signal for an appliance (eg. fire 11) in another house 3.

A control signal (which may be a command or a message signal) suitable for use in the network of Figure 1 is a stream of digits each of which can have any one of three carrier states, namely "high frequency carrier", "no carrier" and "low frequency carrier", represented by "+", "0" and "-" respectively. The digit stream is divided into elements which are pairs of digits. Each digit pair is permitted to have only some of the possible permutations of the carrier states, namely "--", "0+" and "+0" as shown in Figure 2. The elements within a stream are arranged into groups which indicate respectively (see Figure 3) the code of the house to be addressed, the code of the device to be addressed, the encoded data and the encoded control instructions. Clearly the controllers 12, 13 and 14 can each only generate the house address code for that house, 2, 3 or 4 respectively.

Each control signal has an introductory start code of three digits with no carrier, four digits of high frequency carrier, then a single digit of low frequency and one of high frequency to indicate the start of the digit pairs which follow. Each control signal is terminated by three digits with no carrier.

Each of the controllers and each of the appliances has a detector (not shown in Figure 1) capable of determining the carrier state of each digit in any signal received at that unit and hence the permutation of each element. Thus if the detector finds any element with a permutation other than any of those represented in Figure 2, that unit does not accept the control signal containing that element. Moreover from noting the permutation, the detector can determine to a certain extent what the original elements were prior to the collision, using the following table.

Detected Permutation	Original Permutations
0 0	- - : - - (out of phase) 0 + : 0 + " + 0 : + 0 "
+ +	0 + : + 0
- 0	- - : 0 +
0 -	- - : + 0

The interface unit 6' (shown in Figure 4) for light 6 has a microprocessor 17 which analyses each of the signals passing along loop 5 and then takes appropriate action as well as acting as the detector as described above. More specifically, any such signal is fed in through input 18 and then (provided it is in the format of a control signal) it is decoded with microprocessor 17 and a comparison made between the signal's house address code and the code for house 2 which is held in the house code reference unit 19.

If the two codes correspond, ie. the control signal is intended for use within house 2, then a similar comparison is made between the signal's device address code and the code for light 6 which is held in appliance code reference unit 20. Only if these two codes also correspond, will the microprocessor 17 proceed to analyse the data and control sections of the signal and take appropriate action. This may result in, for example, a variation in the power supplied to light unit 6 (by transmission of a signal from output 21) and/or the sending of a return signal to controller 12 indicating the status of light 6. Such a return signal is encoded in separate coder 22 before being fed into loop 5.

In a modification of interface unit 6' for use with a sensing device (e.g. thermostat 9) as distinct from light 6, the processor sends out an appropriate signal from terminal 23 which also acts as an input for the return signal from the sensing device.

In another modification, a second appliance (usually a burglar alarm or hazard alarm) is connected to an interrupt

input 24 of the microprocessor 17 such that if an alarm signal is received at input 24, the microprocessor immediately stops whatever operation it is currently doing, stores the information on that operation and then gives top priority to the transmission of the alarm signals to controller 12.

In another modification, the mains 1 has a master controller which is able to generate and send control signals suitably coded for any or all of the houses. Thus, using a suitable control signal, a gas meter within house 2 can be interrogated and the information on the reading is returned to the master controller. This master controller can generate any of the address codes for the 2, 3 and 4 wherever required.

In any of the situations in which the microprocessor 17 sends a return signal out, it can additionally or alternatively send it to a controller outside the house 2.

In the encoder of Figure 5, parallel binary data is passed along bus 30 and fed into a state machine 31 (to convert it from binary to binary coded ternary) and into state machine 32 (to incorporate carrier signals). Meanwhile another unit 33 (incorporating another state machine, a signal generator and a sequence controller) is suitably regulated in order to insert coding into the processed data via shift registers 34 and 35; thereafter the resultant signal is passed through an FSK modulator 36 and transmission gate 37 to provide its carrier-on form. In Figure 6 there is shown the corresponding decoder in which latch unit 40 is used to accept only those signals with permitted permutations. Thus the arrangement of gate devices within detector unit 41 is designed such that Q of latch unit 40 goes high for a valid signal (thereby allowing conversion unit 42 to convert the data signal) whereas $\overline{Q}$ of latch 40 goes high for an invalid signal (thereby making conversion unit 42 abort conversion of the data signal). Conversion unit 42 corresponds to the reverse arrangement of components within Figure 5.

The network described above can readily be modified to have digits of multiple-states other than ternary (e.g. binary or quarternary) and to have numbers of predetermined, permitted permutations other than three.

CLAIMS

1. A data distribution network having a pathway along which information signals can be sent and a plurality of stations, interconnected by the pathway, for reception and/or transmission of information signals, characterised by the network (1) having means to generate a digital signal for transmission with the network, said signal being formed of a plurality of elements of which at least some are each formed of one of a number of predetermined permutations of multiple-state digits, whereby the combination of two or three different such permutations does not result in any of those predetermined permutations, at least one of the stations having means (6') to detect whether an element in a signal has one of the predetermined permutations.

2. A network according to Claim 1, characterised by the at least one of the stations having means (40) to block any signal which has an element with a permutation other than a predetermined one.

3. A network according to Claim 1 or Claim 2, characterised by having means (40) to determine what part of the signal contains the element(s) and means to identify whether the permutation of the element(s) is a predetermined one.

4. A network according to Claim 3, characterised by having means to send information on the identified permutation to a central control unit for the network.

5. A network according to any one of the preceding claims, characterised by means to determine the original composition, before collision, of data signals which have been detected as including permutations other than the predetermined ones.

6. A network according to any one of the preceding claims, characterised by each element comprising two ternary state digits.

7. An encoder for a data distribution network,

characterised by the encoder being capable of forming a digital signal having a plurality of elements of which at least some are each formed of one of a number of predetermined permutations of multiple-state digits, whereby the combination of two or three different such permutations does not result in any of these predetermined permutations.

8. A signal-collision detector for a data distribution network, characterised by the detector having means to identify the state held by each part of an element in a signal, and means to determine whether the permutation of the states within an element is a predetermined permutation.

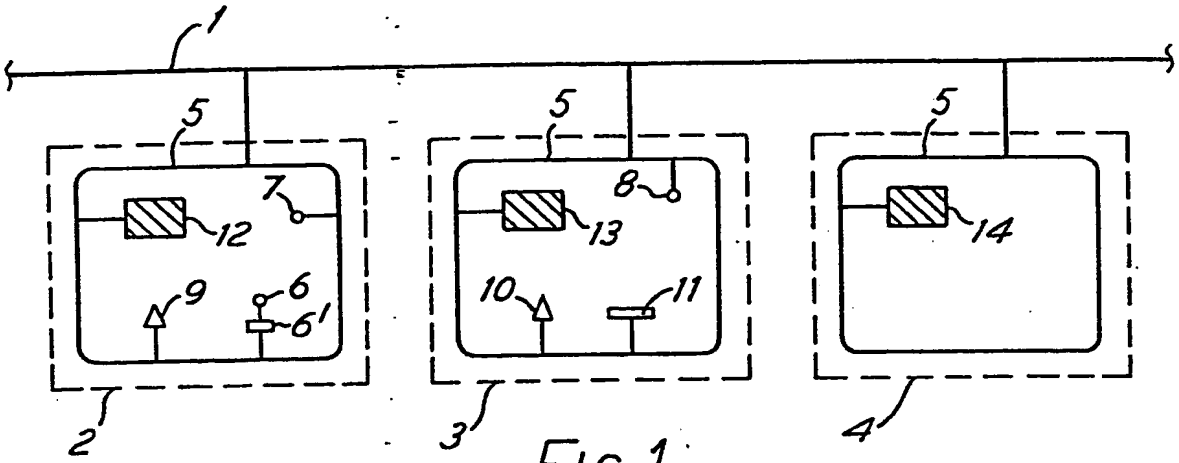

FIG. 1

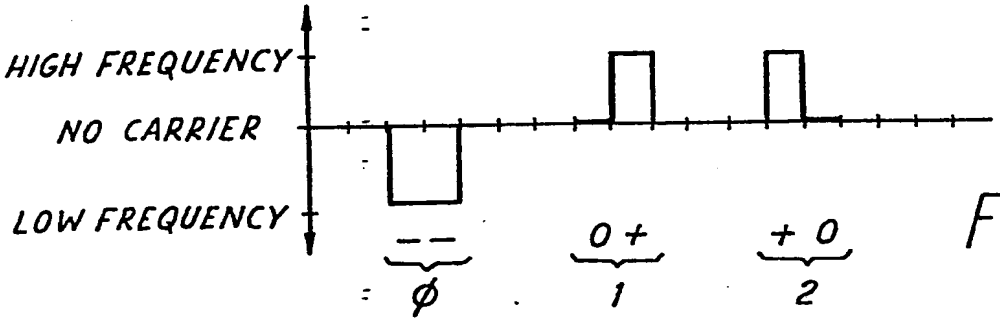

FIG. 2

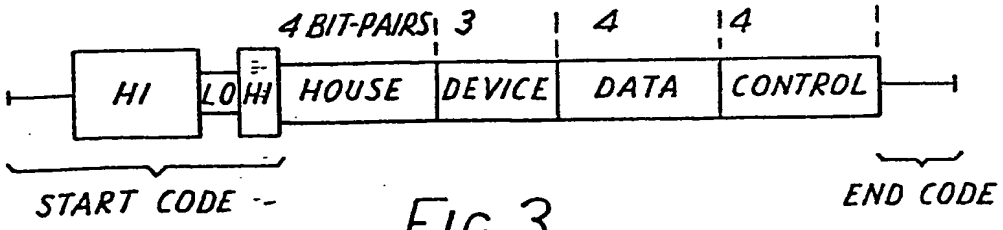

FIG. 3

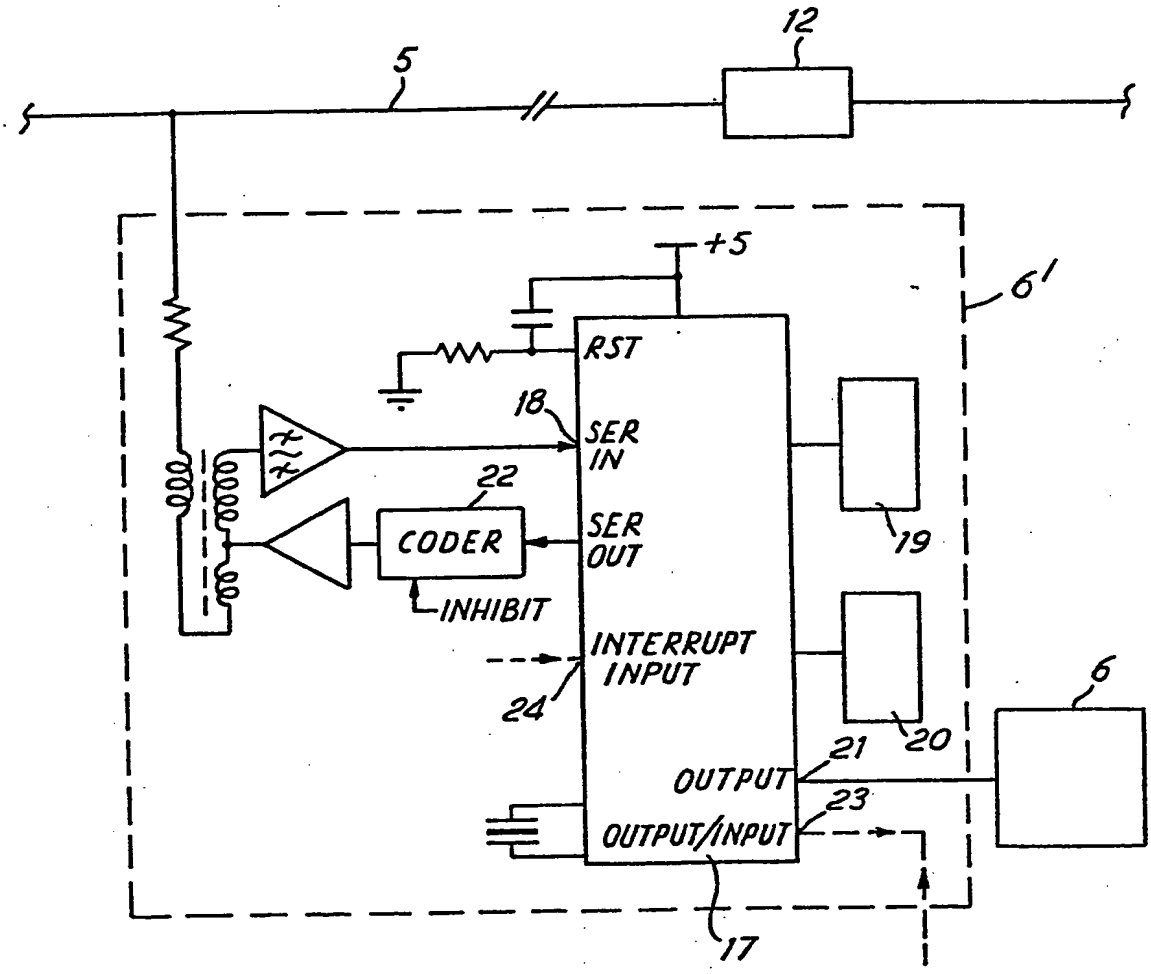
12
5
+5
6'
RST
18
SER IN
22
CODER
SER OUT
INHIBIT
19
INTERRUPT INPUT
24
6
20
21
OUTPUT
23
OUTPUT/INPUT
17

FIG. 4

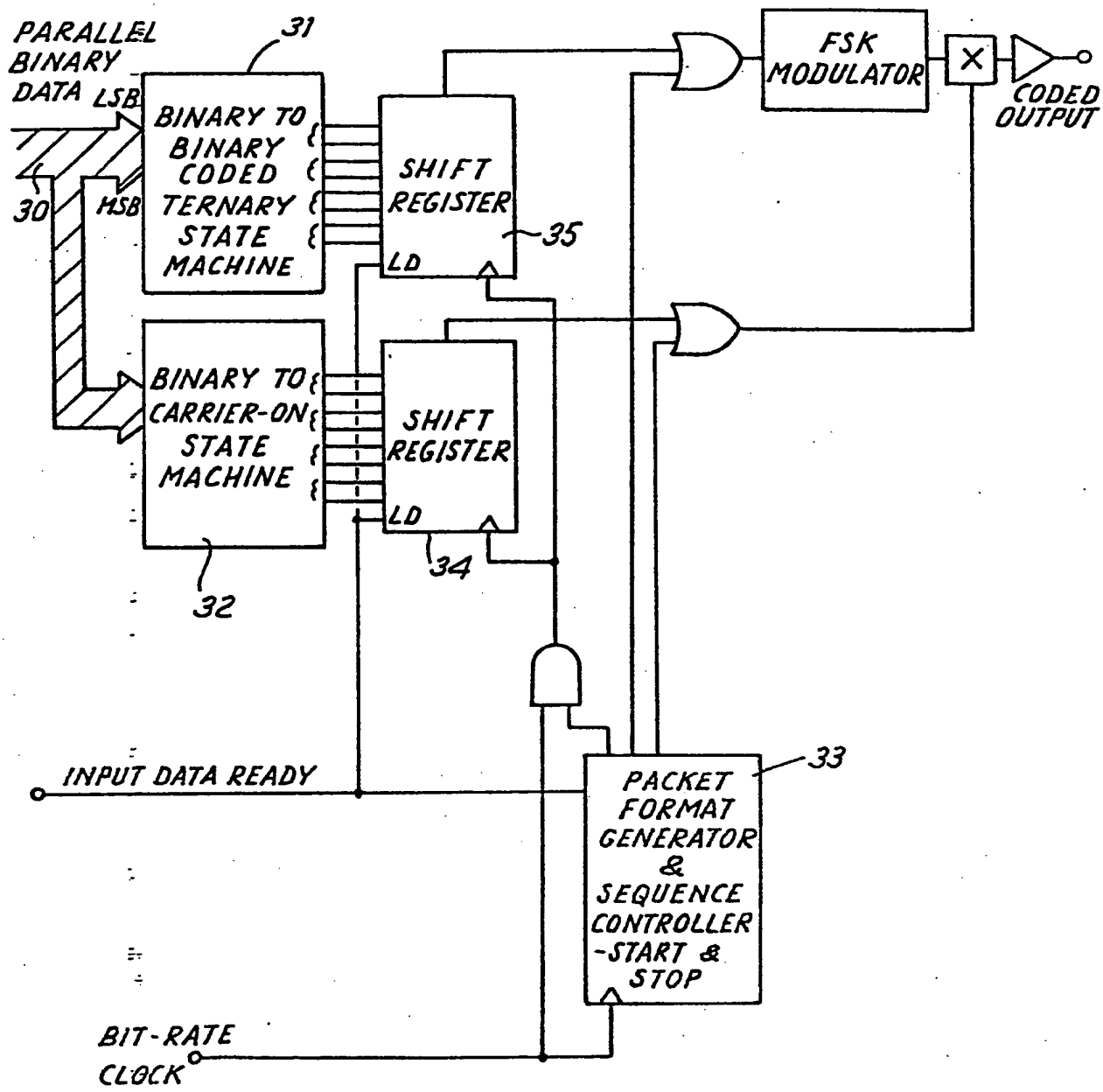
PARALLEL BINARY DATA
LSB
MSB
30
31
BINARY TO BINARY CODED TERNARY STATE MACHINE
SHIFT REGISTER
35
LD
BINARY TO CARRIER-ON STATE MACHINE
32
SHIFT REGISTER
34
LD
FSK MODULATOR
CODED OUTPUT
INPUT DATA READY
33
PACKET FORMAT GENERATOR & SEQUENCE CONTROLLER -START & STOP
BIT-RATE CLOCK

FIG. 5

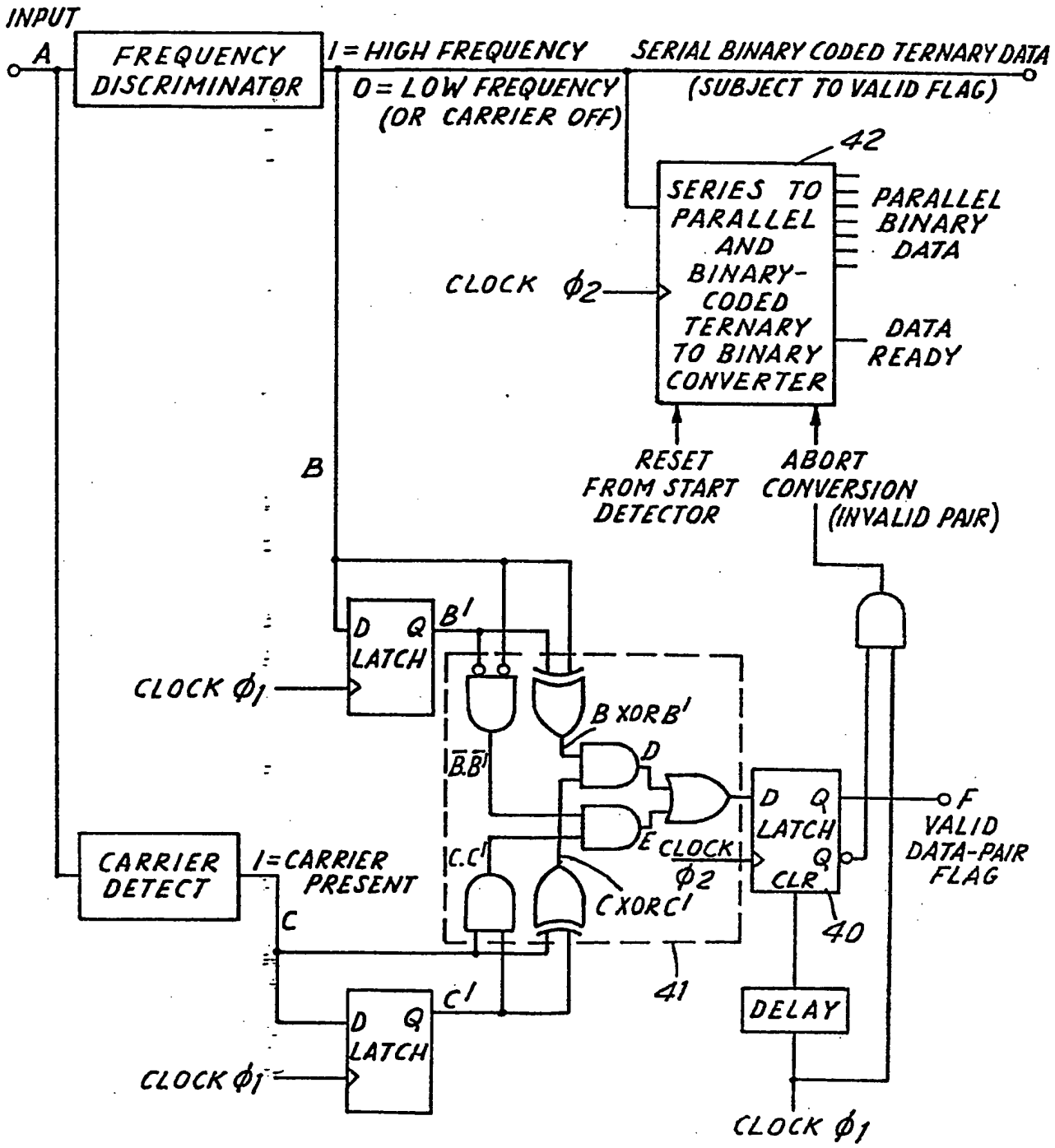
INPUT
A
FREQUENCY DISCRIMINATOR
1 = HIGH FREQUENCY
0 = LOW FREQUENCY (OR CARRIER OFF)
SERIAL BINARY CODED TERNARY DATA (SUBJECT TO VALID FLAG)
42
SERIES TO PARALLEL AND BINARY-CODED TERNARY TO BINARY CONVERTER
PARALLEL BINARY DATA
DATA READY
CLOCK φ2
RESET FROM START DETECTOR
ABORT CONVERSION (INVALID PAIR)
B
D Q LATCH
B'
CLOCK φ1
B XOR B'
B̄.B̄'
D
E
CLOCK φ2
D Q LATCH Q CLR
F VALID DATA-PAIR FLAG
40
CARRIER DETECT
1 = CARRIER PRESENT
C
C.C'
C XOR C'
41
C'
D Q LATCH
CLOCK φ1
DELAY
CLOCK φ1

FIG. 6